A DIGITAL DATA QUALITY MONITOR FOR APPLICATION IN THE NASCOM NETWORK DATA TRANSMISSION SYSTEM

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June 1967

GPO PRICE $ _____
CFSTI PRICE(S) $ _____
Hard copy (HC) 3.00
Microfiche (MF) .65
ff 653 July 65

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Greenbelt, Maryland

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INTRODUCTION

The National Aeronautics and Space Adminstration Communications (NASCOM) Network provides operational communication channels and facilities to transmit mission-related information used in the support of NASA programs and projects. The NASCOM Network provides real-time communication services between all NASA launch centers, mission control centers, computation centers, and domestic and overseas satellite tracking stations. These services are used primarily for real-time command and control of spacecraft.

The NASCOM Network is arranged in a "star" configuration with all overseas services and a majority of the domestic services "hubbing" off the primary communications switching center at the Goddard Space Flight Center in Greenbelt, Maryland. The management and control of all operational Teletype, voice, and high speed data ground communications systems are unified in the NASCOM Network for the support of the Satellite Tracking and Data Acquisition Network (STADAN), the Deep Space Network (DSN) and the Manned Space Flight Network (MSFN). These three networks of tracking stations and associated control centers provide support for unmanned scientific satellites which orbit in space between the earth and the moon, unmanned scientific satellites performing missions to other planetary bodies in our solar system, and manned space flights.

With the ever increasing frequency and duration of missions, the availability of the high speed data ground communication system of 600, 1200, and 2400 bit per second synchronous data must be maximized in order to assure continuous operational mission support. Availability is defined as the probability that the NASCOM Network is operational at any arbitrarily selected time. The capability of monitoring the performance of the high speed data circuits is instrumental in assuring this maximum system availability. The Data Quality Monitor (DQM) is one device that was developed to perform this function.

DESIGN CONCEPT

The equipment engineering design of the DQM, which is based on the process of searching for, verifying and locking on a periodic fixed pattern contained in the incoming data and then detecting bit errors in the pattern, is not a new technique. However, the application of this technique to point-to-point data communication service for detecting errors is unique. It is possible to apply this technique to the NASCOM network because the operational data transmitted is formatted into data frames which contain a fixed and periodic pattern for use in obtaining and retaining frame synchronization for the computers. An example of formatted operational data is the NASCOM Automatic Data Switching System (ADSS) high speed data format which is shown in Figure 1. The frame synchronization words are the two octal 7106 words which are always affixed to all data frames as a header. The rest of the frame varies from one frame to the next and can not be used for the purpose of detecting errors. This format is representative of data formats used in the NASCOM high speed data network.

This digital data pattern containing a known and periodic pattern is available for monitoring at the transmit or receive ends and at the data regeneration stations of the communications circuit. If degradation of the data occurs, the source of this degradation can be easily isolated and the degraded circuit segment can be replaced to make the circuit good.

EQUIPMENT DESCRIPTION

Normal Operation Functional Block Analysis - In normal operation the DQM can be programed to detect errors in any of four predetermined portions of the data block. These predetermined portions and the associated detected errors are (1) bit errors in the frame (block) synchronization words (FSW's), (2) even bit parity errors in data words, (3) odd bit parity errors in data words and (4) data word format errors in three fixed data word formats.

NASCOM ADSS
INTER C.P. HIGH SPEED DATA FORMAT

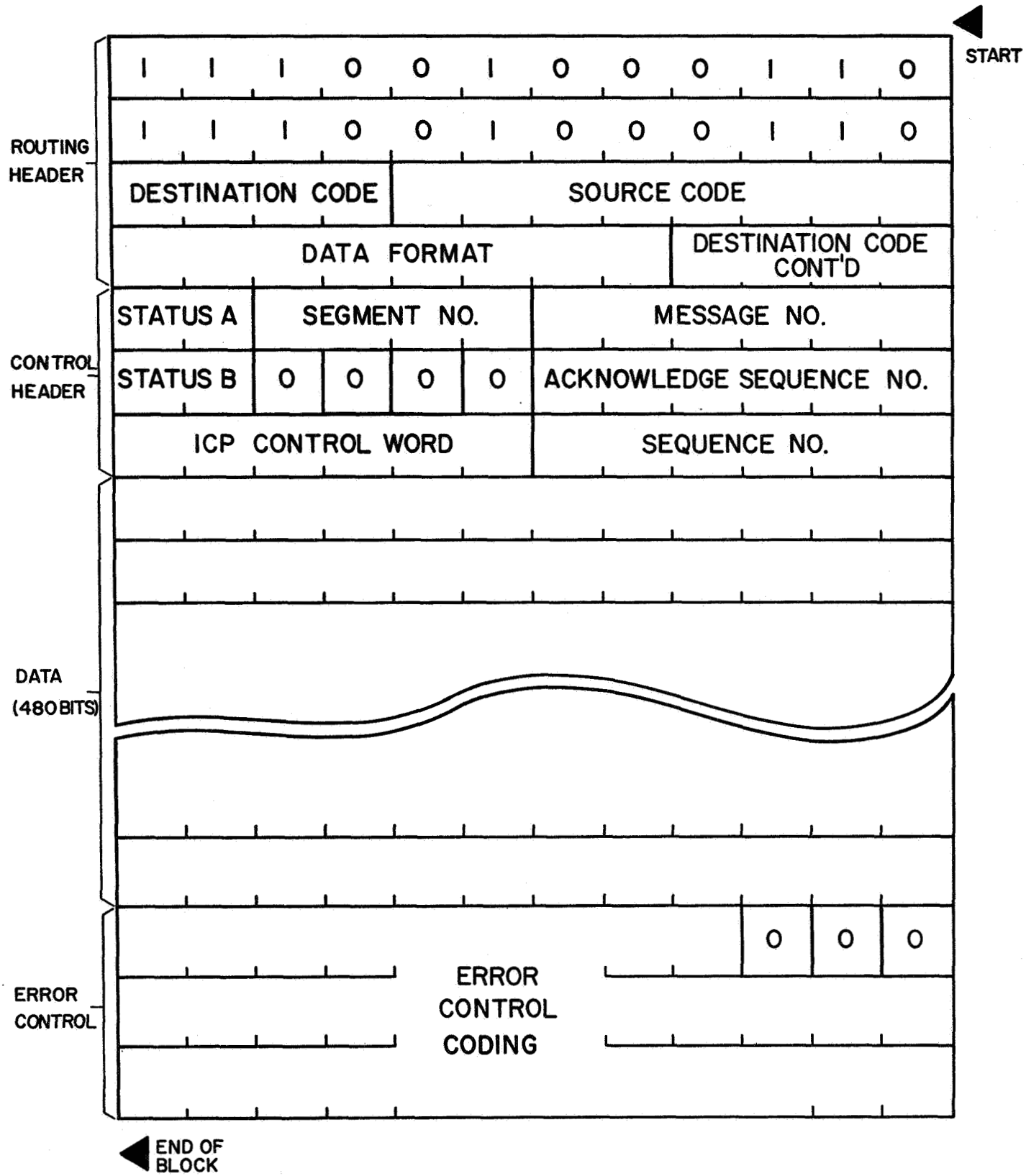
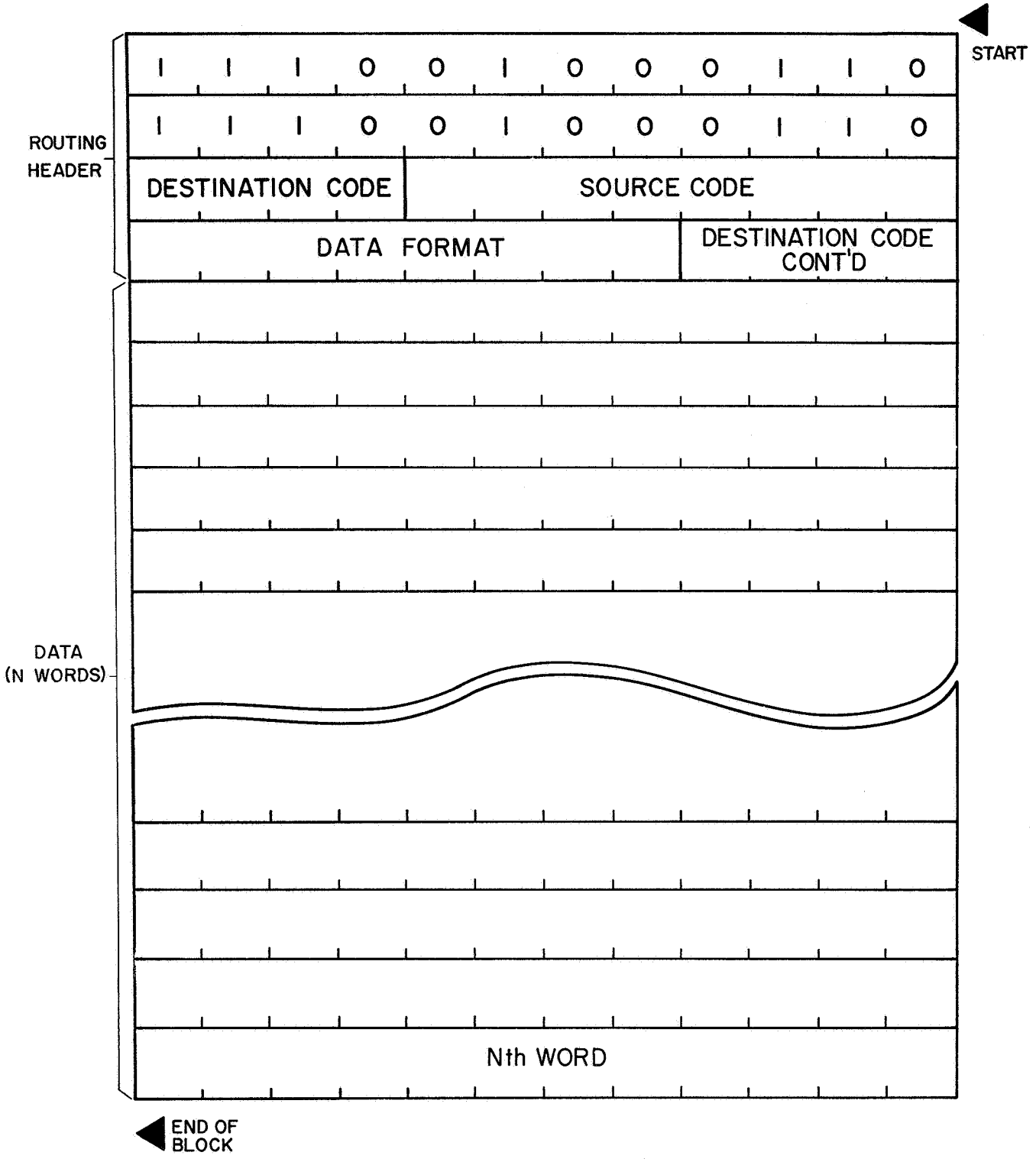


FIGURE I

NASCOM ADSS
BASIC HIGH SPEED DATA FORMAT



The following functional blocks of the DQM comprise the entire logic circuitry necessary to detect the described errors above. Figure 2 and Figure 3 show the functional block diagram of the DQM. Figure 4 and Figure 5 show the DQM with operational program plug and the DQM internal view, respectively.

Power Supply - The power supply operates on 115/230 volts, 50/60 Hz power and provides the eight DC voltages required by the DQM circuitry.

Input Interface and Display - Either front panel or rear panel connections provide the input interface with clock and data inputs. The clock input and data input interface circuits are identical and program connections are used to adapt the input interface for either polar or negative neutral inputs. Each interface circuit accepts either the polar or negative neutral input signal, decides whether the signal is a logical 1 or a logical 0, regenerates the signal, and provides the regenerated signal and its complement (of both data and clock) as outputs.

A front panel switch selects either data or its complement to input the data register. The selection of clock or its complement to input the clock phase and pulse generator is a programable parameter. Selection of clock input defines the bit period as beginning at the negative going transition of the bit clock. Selection of its complement input defines the bit period as beginning at the positive going transistion of the bit clock. Front panel indicators display the logic level of the input data to the data register.

Clock Phase and Pulse Generator - The regenerated clock or its complement is the only input to this circuit. From this regenerated input the clock phase and pulse generator develops the following outputs which are used by the DQM as basic time references.

a. A further regenerated clock and its complement.

b. A pulse at the negative going transition of the regenerated clock, and another pulse delayed from this pulse by the duration of this pulse.

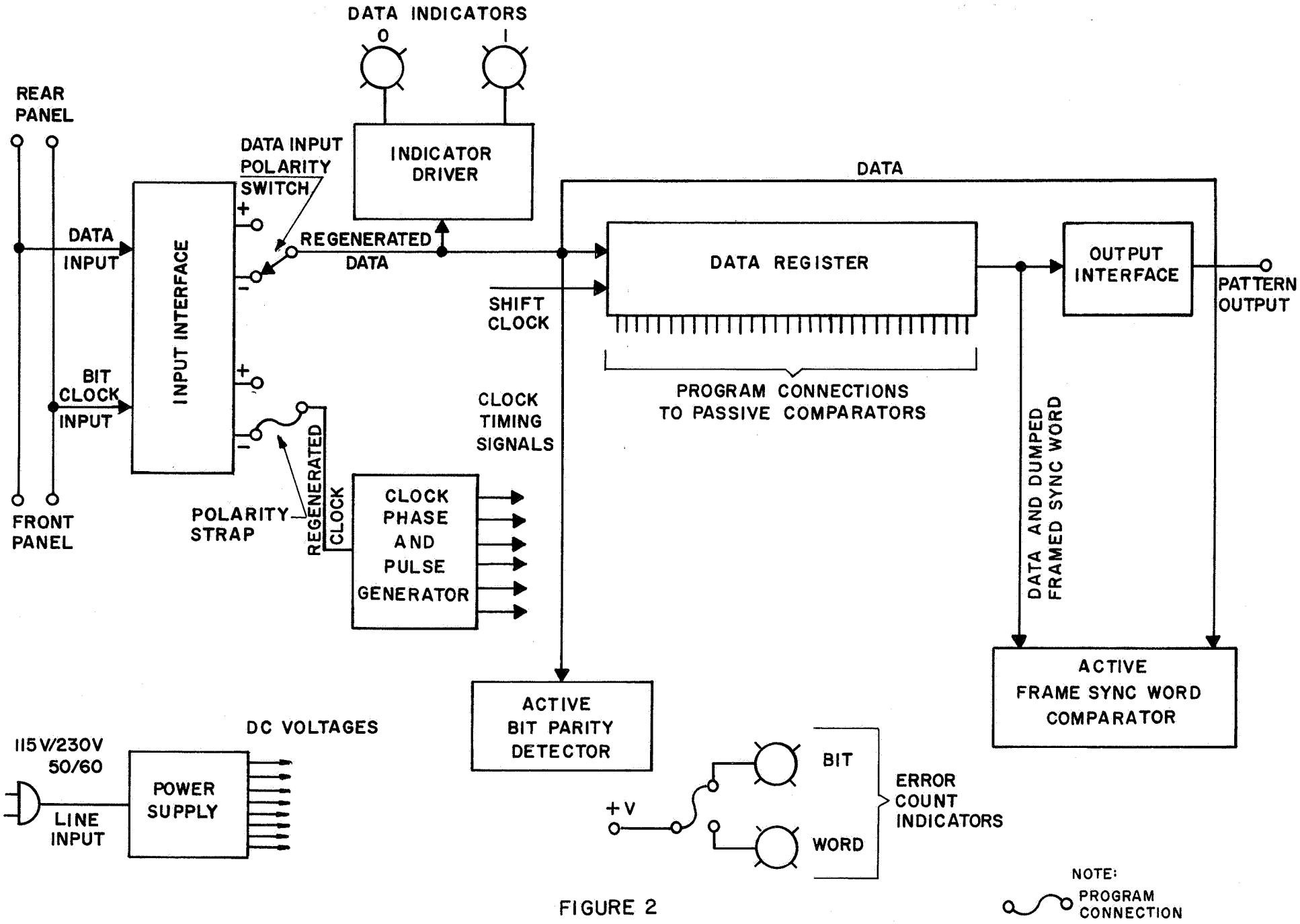


FIGURE 2

DQM FUNCTIONAL BLOCK DIAGRAM

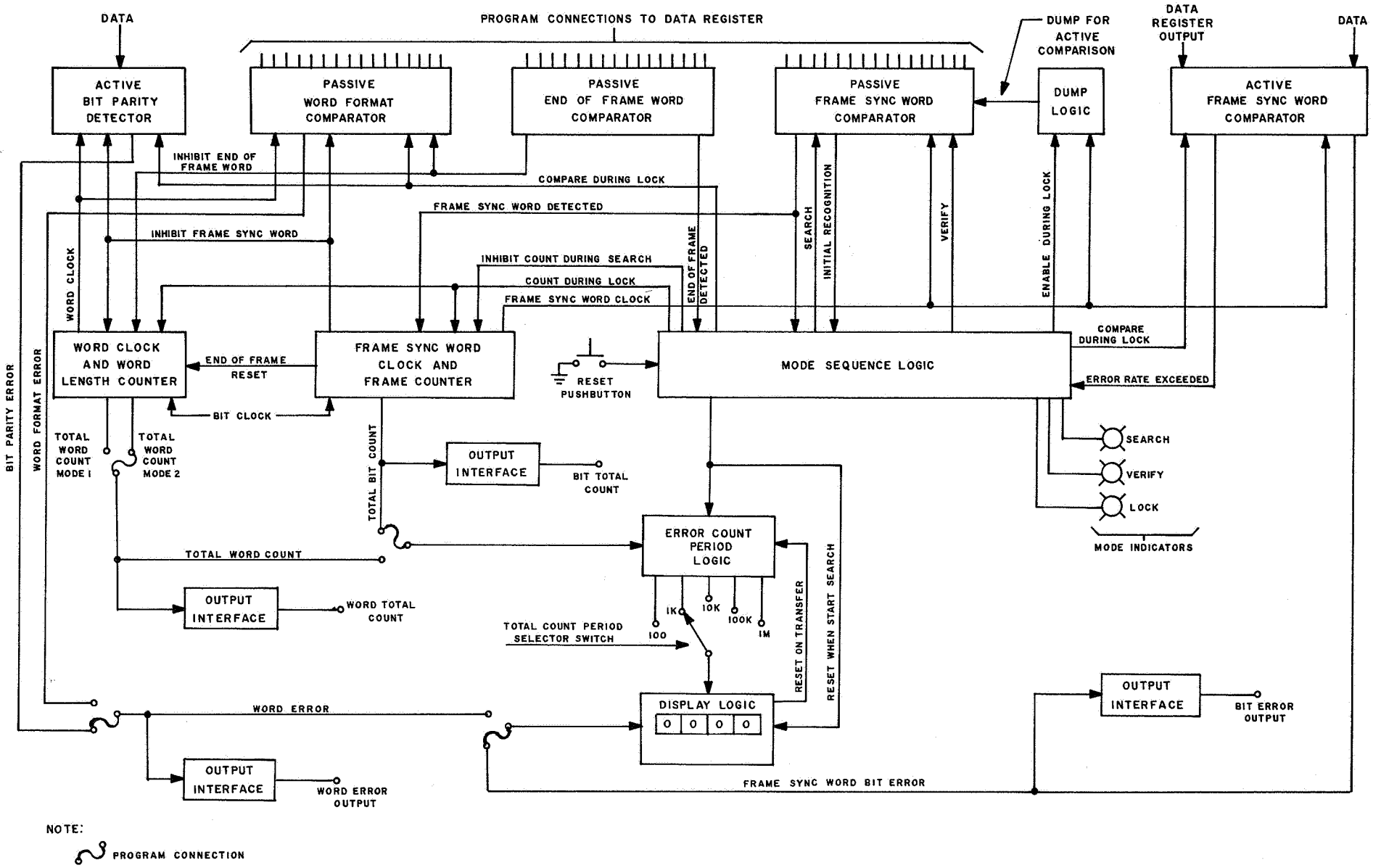


FIGURE 3
DQM FUNCTIONAL BLOCK DIAGRAM(CONT.)

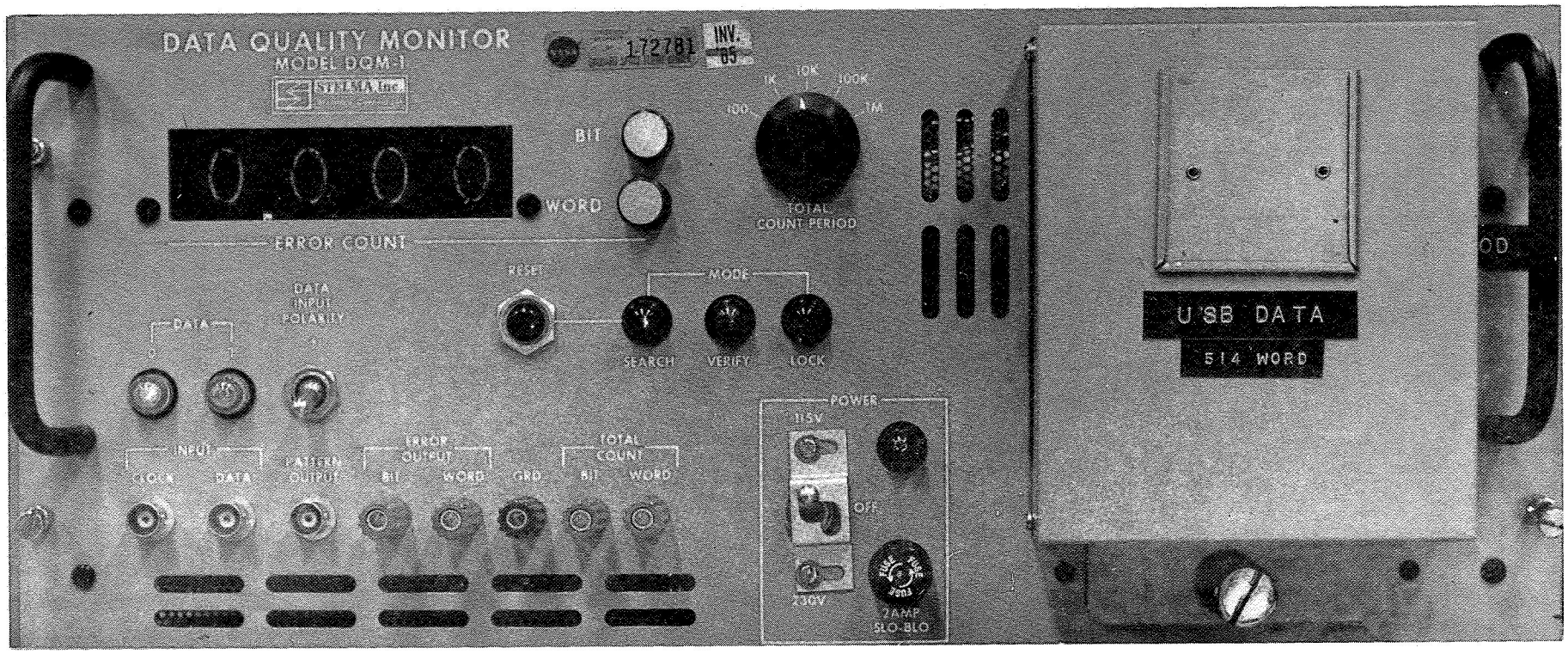


FIGURE 4

DQM WITH OPERATIONAL PROGRAM PLUG

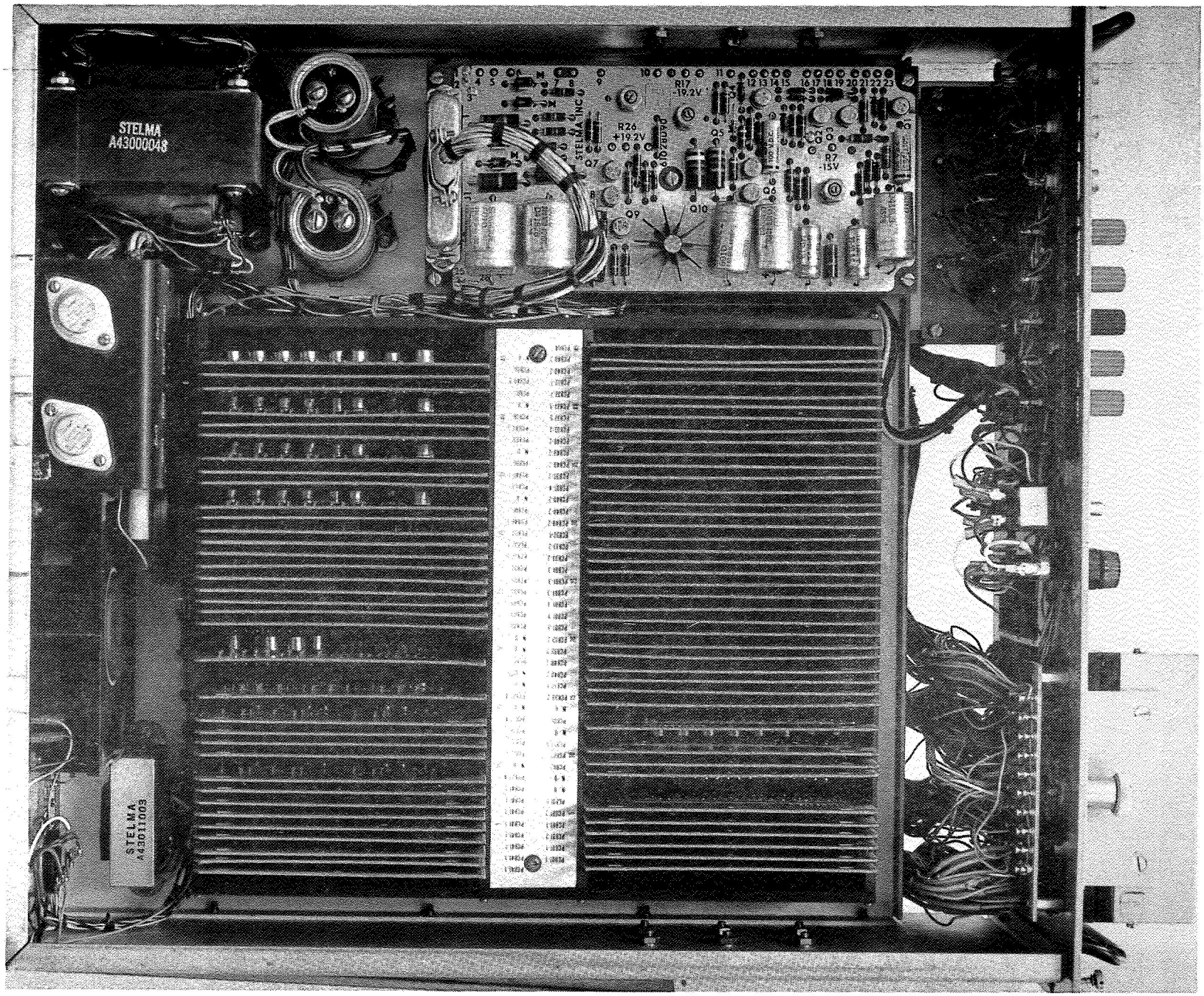


FIGURE 5

DQM INTERNAL VIEW

c. A pulse at the positive going transition of the regenerated clock, and another pulse delayed from this pulse by twice the duration of this pulse.

Data Register - The data register is a 32 bit shift register into which the regenerated data is serially shifted at a rate equal to the input clock. Sixty four parallel outputs representing the set and reset outputs of the 32 stages are provided to the program plug. These outputs are provided through a pre-wired program as inputs to the DQM's three passive comparators. Although the parallel output signals are coupled to passive comparators, they are not necessarily utilized until other logic and timing conditions are met. The serial output of the data register is applied to an output interface where it is amplified and provided as the pattern output.

Passive Frame Sync Word Comparator - When the mode sequence logic reset pushbutton is momentarily depressed, the applied ground forces this logic to the search mode. The mode sequence logic in turn provides a search command to the passive quasi-analog FSW comparator. The comparator now looks continuously at the programmed stages of the data register.

When a true FSW is serially shifted into these programmed stages, the parallel outputs to the comparator are all logical 1's. The comparator recognizes these logical 1's as the initial FSW detection. Since a small degradation of data would prevent this initial recognition, the comparator can allow a programmed number of shift register outputs to be in error. As long as the number of tolerable bits in error meets or exceeds the actual errors, initial recognition is made which forces the mode sequence logic to the verify mode. Detection of the initial FSW also resets the FSW clock and frame counter.

From the time of the initial FSW recognition until the next FSW time, no comparison is made. When the FSW clock indicates that it is time for another FSW to be in the

correct stages of the data register and the mode sequence logic provides a verify command, a comparison is made. If the number of tolerable bits in error meets or exceeds the actual errors, a legitimate FSW is detected. However, should the actual errors be greater than the programmed amount, a detection is not made, and the mode sequence logic automatically cycles operation back to the search mode.

When a predetermined number of legitimate FSW's have been detected, mode sequence logic automatically initiates the lock mode. While in the lock mode, the passive FSW comparator is no longer used for comparison purposes.

Dump Logic - The dump logic is enabled only during the lock mode and is activated by the FSW clock. Just prior to the anticipated (via program connections) arrival of the first bit of the FSW into the data register, the programmed FSW is stored in the register. This is accomplished because, due to program connections to the data register, the passive FSW comparator contains an inherent memory of the programmed FSW. Previously the correct FSW in the data register caused the parallel inputs to the comparator to be all logical 1's. By forcing all of these parallel program lines to logical 1's, the programmed FSW is dumped into the data register.

Active Frame Sync Word Comparator - The active FSW comparator is enabled only during the lock mode and is activated by the FSW clock. The programmed FSW is dumped into the data register just prior to the actual FSW being shifted serially into the data register. As the first bit of the received FSW appears as the input to the first stage of the data register, the first bit of the programmed FSW appears as the output of the last stage of the data register, and both first bit signals are provided to the active FSW comparator.

Thsi comparator, an exclusive OR logic circuit, compares these two first bits, as well as the continuing FSW bits, and detects individual bit errors. The bit error pulse generated is provided to the display logic by a program connection. The bit

error pulse is also provided to an output interface where it is amplifed to appear as the bit error output.

The FSW comparator also generates an internal error tolerance exceeded signal when the FSW bit errors exceed the programmed tolerance. When the programmed number of consecutively incorrect FSW's have been detected (each incorrect FSW being indicated by the error tolerance exceeded signal), an error rate exceeded signal is developed which forces the mode sequence logic back to the search mode. Thus, alternate tolerable and incorrect FSW's may occur and operation remains in the lock mode. Only when consecutive incorrect FSW's detected exceed the programmed tolerance does the DQM operation cycle from the lock to the search mode.

Frame Sync Word Clock and Frame Counter The FSW clock and frame counter is inhibited until an initial FSW is detected. The counter is enabled during the verify and lock modes and counts total bits to the beginning of the FSW and total bits to the end of the FSW. The gate developed from these two functions represents the time during which the FSW begins to enter the data register until the time it starts to exit the register. The time just prior to the FSW entrance into the register is the time the programmed FSW is dumped into the register. The time just prior to the FSW exit from the register is the time the entire FSW is stored in the register and a passive FSW comparison is made. The entire time between the two functions is the time active FSW comparisons are made.

The FSW clock and frame counter also provide the following functions:

a. End of frame reset to the word clock and word length counter.

b. An inhibit signal for various error counts and total counts.

c. Total bit count of all FSW bits checked by the active FSW comparator. This total bit count is provided to the error count period logic by a program connection. This count is also provided to an output interface where it is amplified to appear as the bit total count output.

Word Clock and Word Length Counter - The word clock and word length counter counts only during the lock mode. It is inhibited by an end of frame word (EOFW) detection and is reset at the end of frame time. The output word clock signal is used to time bit parity and word format checks. Two other outputs are designated total word count mode 1 and total word count mode 2. The mode 1 word count is a count of all words or a count of all words except FSW's (selection is programable). The mode 2 word count is a count of all words except the FSW and the EOFW. Either output may be selected by program as the input to the error count period logic. The total word count signal is also provided to an output interface where it is amplified to appear as the word total count output.

Passive End of Frame Word Comparator - This comparator is the same type (quasi-analog) as the passive FSW comparator, except that it performs no dump function and operates at all times. Through program connections it is connected to either the set or reset output of selected stages of the data register. It detects an EOFW when all or a tolerable number of the stage outputs are logical 1's. Upon detection, the mode sequence logic is forced to the search mode, and word format checks and total word counts are inhibited.

Active Bit Parity Detector - The active bit parity detector is essentially a flip-flop which changes state for every input data logical 1. By enabling the detection during the lock mode, and resetting the flip-flop by the word clock at the end of the word time, the set and reset outputs are complementary and represent either an even parity or an odd parity. Either even parity or odd parity checks may be programmed. The bit parity check of the FSW can be inhibited by a program connection. The bit parity error output represents odd or even bit parity errors of all words, or of all words except the FSW.

Passive Word Format Comparator - The passive word format comparator contains three

multiple input NANS gate circuits which are connected by program connections to either the set or reset output of various stages of the data register. With the DQM in the lock mode and a data word (excluding FSW and FOFW) stored in the data register, a comparison between this word and each of the three programmed data words is made. When the word in the register compares exactly to one of the programmed words, all data register stage outputs are seen by one of the NAND gates as logical 1's and no word format error is developed. Only if the stored data word does not compare to at least one of the three programmed words is a word error developed.

Mode Sequence Logic - Most of the functions performed by this logic have been previously described. This logic circuitry senses various system parameters, determines which mode the DQM should operate in, and provides various enable and inhibit signals throughout the system.

The search mode is initiated by any of the following conditions:

a. Depressing the reset pushbutton.
b. Lacking a consecutive detection of a legitimate FSW in the verify mode.
c. Exceeding the tolerable FSW error rate in the lock mode.
d. Detecting a legitimate EOFW.

The verify mode is initiated by the first detection of a legitimate FSW. The lock mode is initiated by detecting a programmed number of consecutively FSW within the programmed tolerance when in the verify mode. Through program connections the verify mode can be bypassed. The first detection of a legitimate FSW in the search mode would automatically initiate the lock mode.

Three front panel indicators identify the mode in which the DQM is operating.

Error Coutn Period Logic - This logic is enabled during the lock mode and through program connections counts either the total bits that are compared by the active

FSW comparator or the total word count. Five count signals (100, 1K 10K, 100K, 1M) are presented as outputs.

Display Logic - This logic counts either FSW bit errors or word errors. At the end of a count period (determined by which count signal from the error count period logic inputs the display logic) the number of errors counted from the initiation of the count period is displayed by the digital read-out. This count is held until another count period is terminated, at which time the total number of errors counted during this period is displayed.

Output Interface

a. Recording Outputs. The following are available as pulse outputs during the lock mode:
   1. Bit Error Output. Provides output connections for bit errors between input data FSW and programmed FSW.
   2. Word Error Output. Provides by program output connection for either (a) odd or even bit parity errors of all words, (b) odd or even bit parity errors of all words except FSW, or (c) data word format errors.
   3. Bit Total Count. Each output pulse represents one bit of the FSW that is being checked for validity.
   4. Word Total Count. Each output pulse represents one data word that is being checked for validity.

b. Data Register Output. During the search and verify modes, this output provides the regenerated input data. During the lock mode, this output represents the regenerated input data except for some data word bits preceding the input FSW. The programmed FSW appears in the place of these data word bits.

c. Error Count Indicators. A bit or word error count lamp indicates which type of error is being displayed by the digital read-out.

Programable Parameters - All programable parameters necessary for operation of the DQM to detect bit errors or word errors are described below.

Required Program Connections

a. Disable 9 + 11 pattern generator, thus enabling data to be shifted into the data register.

b. Enable an active bit-by-bit comparison of the FSW during lock mode.

c. Enable the programmed FSW to be dumped into the data register only in the lock mode.

d. Enable error count period logic only during lock mode.

e. Reset error count display when operation cycles to search mode.

Input Interface Program Connections

a. Data - negative neutral or polar.

b. Clock - negative neutral or polar; define bit period to begin at either negative going or positive going transition of bit clock.

Frame Length Program Connections - 1 to 4096 bits.

FSW Program Connections

a. Lenth - 1 to 32 bits

b. Configuration - any combination of logical 1's and logical 0's.

Data Word Program Connections

a. Length - 1 to 32 bits.

b. Occurrence - a definite number of bits after the FSW.

FSW Detection Tolerance Program Connection - 0 to 16 bit errors in search and verify modes only.

EOFW Program Connections

a. Length - 1 to 32 bits.

b. Configuration - any combination of logical 1's and logical 0's.

c. Tolerable bit errors - 0 to 16 errors.

Mode Cycling Program Connections

a. Enable operation in search, verify, and lock modes, Cycles from verify to lock after a programmed number of consecutively correct (within programmed tolerance) FSW's have been detected.

b. Enable operation in only search and lock modes. After one legitimate FSW detection in the search mode, the lock mode is automatically initiated.

Verify Mode Count Program Connection - Number (0 to 7) of consecutively correct (within FSW detection tolerance) FSW's that must be detected before lock mode is initiated.

Lock Mode Error Tolerance Exceeded Program Connection - Number (0 to 30) of FSW bits if in error during the lock mode comparison cause recognition of an illegitimate FSW.

Lock Mode Error Rate Exceeded Program Connection - Number (0 to 14) of consecutively illegitimate FSW's which cause recycle to search mode.

Bit Parity Program Connections

a. Odd bit parity check.

b. Even bit parity check.

c. Exclude or include FSW in bit parity check.

d. Exclude or include FSW in total word count.

Word Format Program Connections

a. Three word patterns.

b. Each word pattern 1 to 32 bits in length.

c. Any logical 1 and logical 0 configuration for each word pattern.

Output and Display Program Connections

a. Provide either (1) bit parity errors of all words or all words except FSW, or (2) word format errors to word error output jack.

b. Provide either (1) total count of all words or all words except FSW, or (2) total count of all words except FSW and EOFW to word total count output jack.

c. Enable either (1) signal to word error output jace or (2) signal to bit error output jack to be displayed by the digital read-out.

d. Enable either (1) signal to word total count output jack or (2) signal to bit total count output jack to be used as the input for the error count period logic.

e. Enable either (1) front panel bit error count indicator or (2) front panel word error count indicator.

Internal Test Modes - The DQM contains four programable internal test modes which are self-checking features to indicate the unit's operability. Figure 6 shows the simplified test mode block diagram of the DQM. In these four test modes the DQM considers an internally generated pseudo-random pattern at the input bit clock rate as the input data. This internal pseudo-random pattern is a 2047 bit pattern which is generated by an exclusive OR function of the 9th and 11th stages of the data register. A 32 bit known configuration within this pattern is designated as the FSW. The remaining portion of the pseudo-random pattern represents sixty-five 31 bit data words. The pseudo-random pattern generator is continuously enabled by a test program plug, which also provides selection of the internal test modes. Figure 7 shows the DQM with the test program plug.

When the DQM is in any one of the internal test modes, the unit automatically cycles through the search and verify modes until the lock mode is achieved. Capability to reach the lock mode indicates over-all unit operability, tolerable FSW detection and

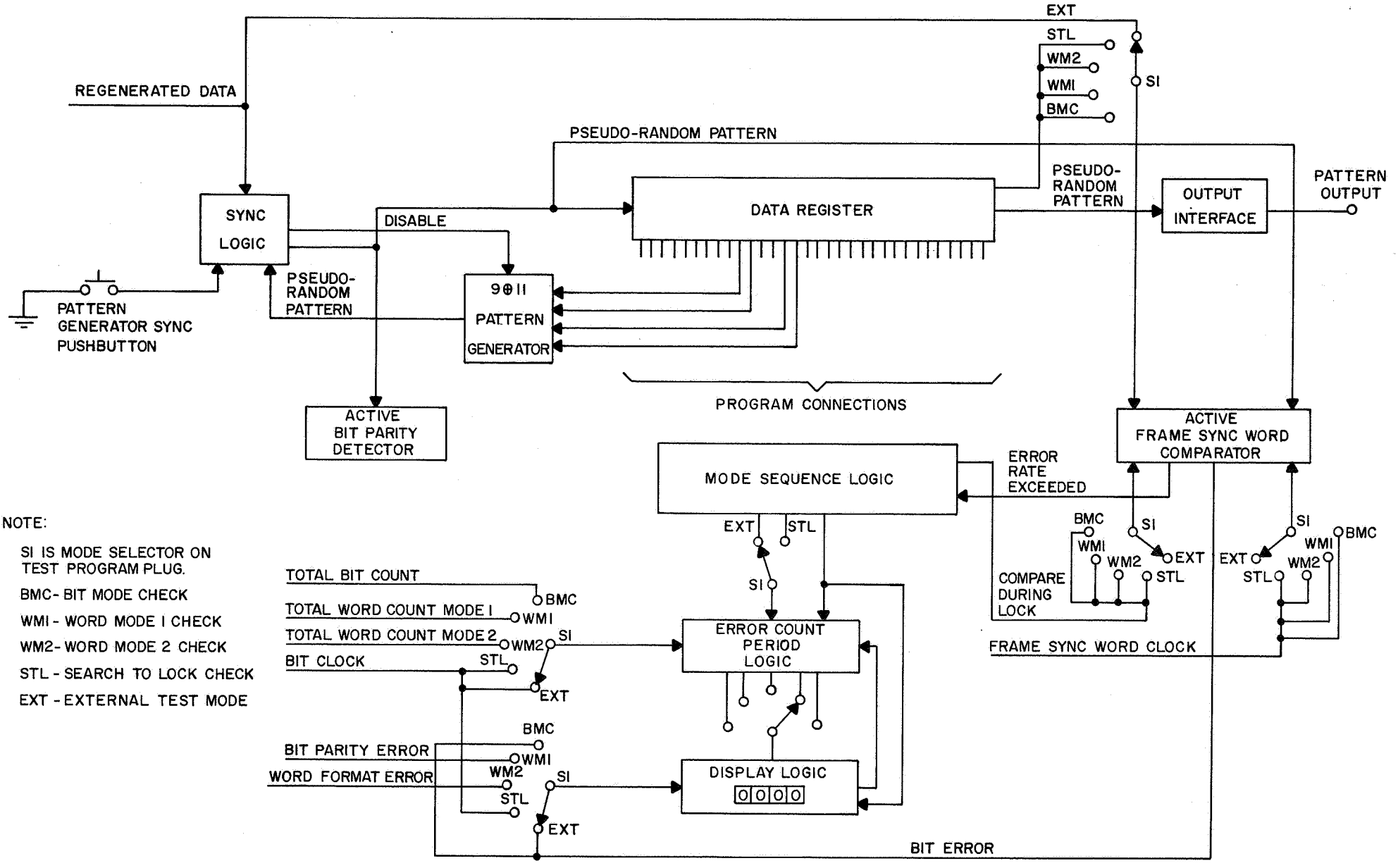


FIGURE 6

DQM SIMPLIFIED TEST MODE BLOCK DIAGRAM

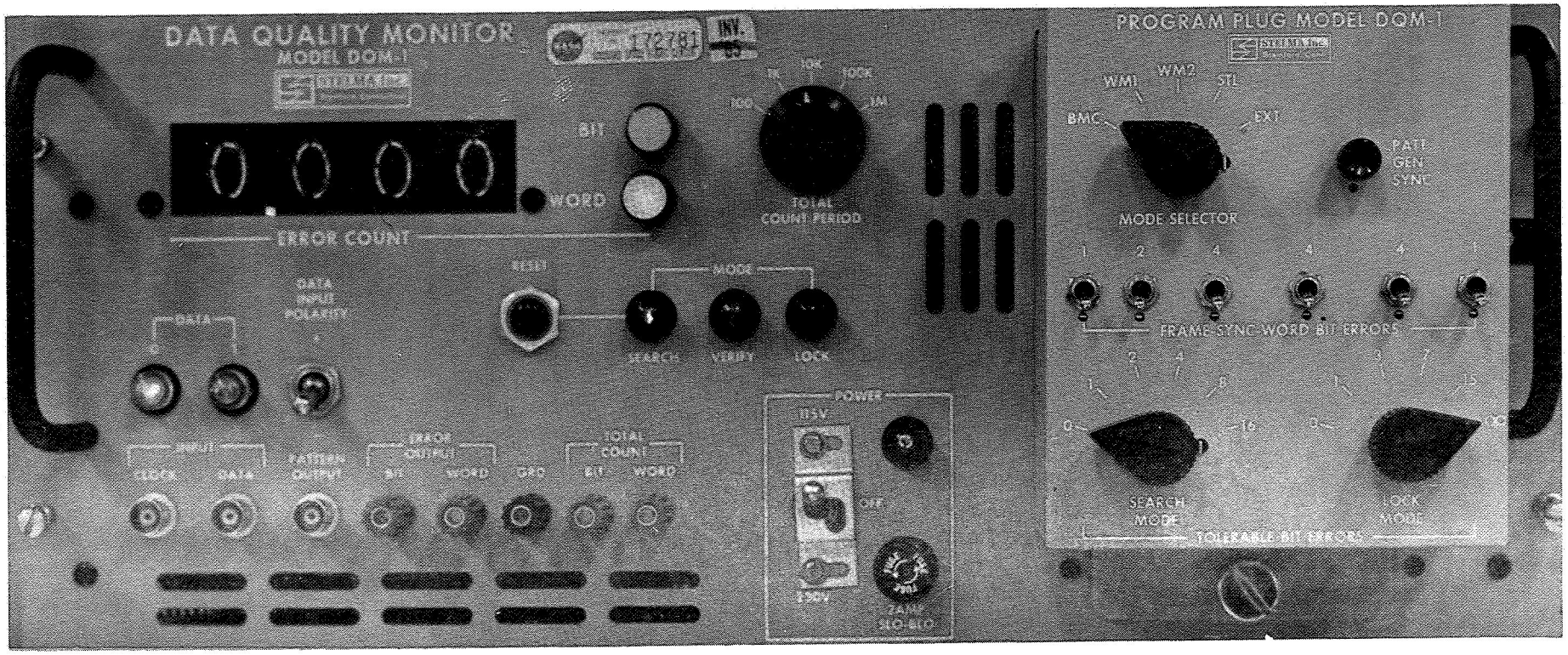


FIGURE 7

DQM WITH TEST PROGRAM PLUG

satisfactory mode cycling. The test program plug allows intentional bit errors to be inserted in the FSW recognition circuitry, and allows selection of tolerable FSW bit errors in the search and lock modes.

The digital read-out is enabled, when lock mode is reach, to display the results of any one of the four further described internal checks. These digital read-outs further indicate individual circuit as well as over all unit operability.

Bit Mode Check - The FSW of the pseudo-random pattern is compared by the active FSW comparator on a bit-by-bit basis to the inverse of the 32 bits preceding the FSW. Fifteen bit errors exist in this comparison. A specific number of errors should be indicated by the digital read-out when all bit comparison logic is functioning properly. During all internal test modes, the bit errror output represents these bit errors.

Word Mode 1 Check - In this test mode the active bit parity detector is programmed for an odd bit parity check. Each pseudo-random pattern data word is checked for an odd parity. The first 100 pseudo-random pattern data words contain 52 odd bit parity errors (even bit parity). A specific number of odd bit parity errors should be indicated by the digital read-out when all parity error detection logic is functioning properly.

Word Mode 2 Check - In this test mode the passive word format comparator is programmed for two of the pseudo-random pattern data words. Word format checks are performed on this pattern. Ninety-six word format errors exist for the first one hundred pseudo-random pattern data words. A specific count is indicated by the digital read-out when all word format detection logic is functioning properly.

Search To Lock Check - In this test mode bit clock is provided to the error count period logic and the display logic. The digital read-out displays the total count of all bits checked from int initiation of the search mode to the enabling of the

lock mode, and indicates that the error count period logic and display logic is functioning properly.

External Test Mode - In this test mode an input pseudo-random pattern and input clock arequired. To synchronize the internally generated pseudo-random pattern with the external pattern, the internal pattern generator is disabled and the external pattern is shifted into the data register. When DQM operation has cycled to the lock mode, the internal pattern generator is enabled. Since the data in the register is synchronous with the external pattern, internal pattern generation is continued synchronously with the external pattern.

The external and internal patterns are applied to the active FSW comparator. The signals which normally inhibit an active FSW comparison in search and verify modes, and enable a comparison only during the FSW time are not used in this test mode. Thus a continuous bit-by-bit comparison is enabled. Bit clock is provided to the error count period logic. Bit errors between the internal and external patterns are provided to the digital read-out and the bit error output.

The pattern output of the DQM is the pseudo-random pattern when the unit is operating in any of the test modes.

SYSTEM APPLICATION

It is planned to use a total of fifty-eight DQM's in the NASCOM Network at switching centers, HF radio/wireline regeneration stations and MSFN. At the present time it is not possible to use the DQM in the STADAN and DSN because some of the data formats of these networks are arranged such that it is impossible for the DQM to lock on any portion of the data stream and they do not use the 24 bit header previously mentioned.

In the MSFN the DQM has proven to be extremely useful in isolating system troubles during network simulations and checks. Simulations are testing programs where all parts of the ground network are exercized using simulated data for the purpose of proving its capability of supporting a mission prior to the mission. Certainly, the task of integrating several computer systems spread all around the world is a very complex problem. The DQM aids in simplifying this problem by segmenting the system into discrete subsystems. The following example will help to clarify this point.

Assume that tracking and telemetry data are to be transmitted from the MSFN site at Carnarvon to the real-time computers at Houston, Texas. This system is made up of the tracking and telemetry computers at Carnarvon, the 2400 bit per second high speed data communication transmission subsystem with data regeneration at Canberra and Honolulu switching centers, main switching computer at GSFC, a 40.8 kilobit per second wideband transmission subsystem and the computers at the Mission Control Center at Houston.

First, consider the sequence of events when there is no DQM in the system and bad data is being received at Houston. The controller at Houston informs the controller at the main switching computer at GSFC of the difficulty. The switching computer controller at GSFC checks some lights on the computer display which indicate to him that the data input and output is satisfactory; so the difficulty is passed on to the communication controller at GSFC who listens to the audio tones on the circuit and observes on the oscilloscope that there is something present that looks like data. A similar check of

the audio and digital side of the circuit by the communication controllers at the Honolulu and Canberra switching centers is then performed. If there is no indication of difficulty thus far, it is passed on to the computer controller at Carnarvon.

Of course the source or sources of difficulty could lie in the hardware or software of the computers at arnarvon; the data sets at Carnarvon, Canberra, Honolulu, Goddard or Houston; the voice/data circuit segments; the hardware or software of the main switching computer at GSFC; the wideband channel and in the hardware or software of the computers at Houston. Where does one begin to find the difficulty? Note how the DQM aids in isolating the difficulty to a subsystem by its capability of locking on the twenty-four bit frame synchronization word.

If the computer at Houston is unable to input data, but the DQM at the GSFC technical control facility is able to lock on the data, this points to the hardware or software of the Houston computer or the switching computer at GSFC or the wideband data transmission subsystem between Goddard and Houston as the most likely source of difficulty. However, if the DQM is not able to lock on the data or exhibits a high error rate, while the DQM's at Honolulu, Canberra, or Carnarvon lock in on the data, this points to a specific segment of the high speed data circuit as the source of difficulty. If the DQM at the Carnarvon cannot lock in on the data, it points to the hardware of software of the computer at Carnarvon as the most likely source of difficulty. Of course this could also indicate the possibility of an incorrect system configuration such as a tracking data circuit mixed up with the telemetry circuit.

Not only has the DQM been useful in aiding in the interfacing of subsystems but within the NASCOM Network it has been valuable at the HF radio/wireline regeneration stations. At these stations there is an HF modulator-demodulator (modem) designed specifically for transmission of high speed data over HF radio. This modem is operated back to back on the digital side with a wireline data set designed specifically for transmission of high speed data over voice/data quality wireline circuits.

In the testing of these HF radio circuits with the 2047 bit pseudo-random pattern the DQM has been used at the regeneration stations as a means of observing the frequency and the magnitude of the error bursts. By connecting a counter to the DQM the errors can be totaled at the same time the error bursts are being observed so as to provide an overall average bit error rate. By analyzing the error distribution of HF radio circuits in this manner the efficiency of transmitting blocks of data can be determined.

When the regeneration stations begin passing operational data the DQM will afford the operators at the stations the capability of monitoring the quality of the data service being provided by monitoring the quality of the frame synchronization word of the data. As operators and engineers become familiar with the capability of the DQM, more and more ways of using it will become evident. One such application which is presently under study is an engineering analysis of the block error rate of the NASCOM circuits. Presently the performance of the high speed data circuits are evaluated in terms of average bit error; whereas the flight controllers are primarily concerned about the block error rate and the distribution of blocks in error. By using the DQM to provide block error rate performance it is hoped that the determination as to which circuits are usable will be more meaningful.

Another application in which the DQM will probably prove useful is in an engineering study of bit error distribution on NASCOM circuits. The immediate goal of this study is to derive an optimum block length for maximum efficiency of high speed data transmission.

CONCLUSIONS

The DQM has met all the original design requirements. It has proved effective in monitoring the performance of operational high speed data circuits and useful in isolating data circuit segments that have become degraded. Isolating these degraded circuit segments and replacing them with other available circuit segments assures maximum availability of the high speed data portion of the NASCOM Network.

The DQM is NASCOM's initial effort in providing equipment for monitoring the performance of data circuits while passing operational data. Further engineering effort is underway to provide other means of monitoring the quality of live 2400 bit per second digital data traffic.